Nano Scale Disruptive Silicon-Plasmonic Platform for Chip-to-Chip Interconnection

Definition of chip-to-chip interconnection system environment and specification

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Deliverable Responsible

Organization: Athens Information Technology
Contact Person: Emmanouil-P. Fitrakis
Address: Athens Information Technology
19.5 Km Markopoulo Avenue
19002 Peania, Attiki
Greece
Phone: +30 210 668 2721
Fax: +30 210 668 2703
E-mail: mfitrakis@ait.gr

Executive Summary

This document describes the actions that were taken in the context of Milestone 1 for the definition of the chip-to-chip interconnect system.

Change Records

Version	Date	Changes	Authors
0.1 (draft)	2012-01-27	Start	Emmanouil-P. Fitrakis (AIT)
1 (submission)	2012-05-7	Rewrite	Emmanouil-P. Fitrakis (AIT) I. Tomkos (AIT)

Contents

Actions taken with respect to MS1 on definition of chip-to-chip interconnect system environment and specification.

This milestone concerns analyzing and understanding requirements and needs of chip-to-chip communication for systems split over more dice.

In this context, deliverable 2.1 was prepared and submitted to the Project Coordinator (KIT) by ST (lead beneficiary for deliverable) on 1/31/2012, in accordance with the NAVOLCHI Description of Work. AIT also contributed to the analysis.

The contacted analysis will lead to the specification of suitable architectures of the systems, a proper microarchitecture of a Die-to-Die Communication Module (DDCM) and an accurate characterization of the performance required for the physical layer (PHY). This last point will be key to the specification of the plasmonic interconnect in order to meet the chip-to-chip communication required performance.